VII   EC, EE, ML

USN | | | | | | | | | | 06EC71

Seventh Semester B.E. Degree Examination, June/July 2013
Computer Communication Networks

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1   a. Explain briefly with relevant examples, the four levels of addresses that are used in an internet employing the TCP/IP protocols. **(10 Marks)**
    b. Briefly describe the functions of physical layer and data link layer. **(06 Marks)**
    c. Explain the operation of ADSL using 'Discrete Multitone Technique' indicating the different channels, with a diagram. **(04 Marks)**

2   a. Explain the mechanism of selective repeat ARQ with diagram showing send window and receive window. **(10 Marks)**
    b. With suitable block diagram, explain the stop and wait protocol, for noise less channels. Also write the sender site algorithm. **(06 Marks)**
    c. Perform bit stuffing and unstuffing on the given bit stream: 0001111111001111101000. Assume flag as 01111110. **(04 Marks)**

3   a. Explain how collisions are avoided through use of 'IFS, contention window and acknowledgments' in CSMA/CA. With the help of the flow chart show the procedure for CSMA/CA. **(10 Marks)**
    b. Explain 'Token Passing' method of controlled access of the channel. **(06 Marks)**
    c. A slotted ALOHA network transmit 200 bit frames using a shared channel with a 200 kbps bandwidth. Find the throughput if the system produces i) 1000 frames per second ii) 500 frames per second iii) 250 frames per second. **(04 Marks)**

4   a. List the goals of fast Ethernet. Explain the features of physical layer in fast Ethernet. **(10 Marks)**
    b. Explain two different kinds of services as defined in IEEE 802.11. **(06 Marks)**
    c. Write a note on Piconet and Scatternet in Bluetooth. **(04 Marks)**

PART – B

5   a. A system with four LANs and five bridges is shown in Fig.Q5(a). Choose B1 as the root bridge. Show the forwarding and blocking ports, after applying the spanning tree procedure.
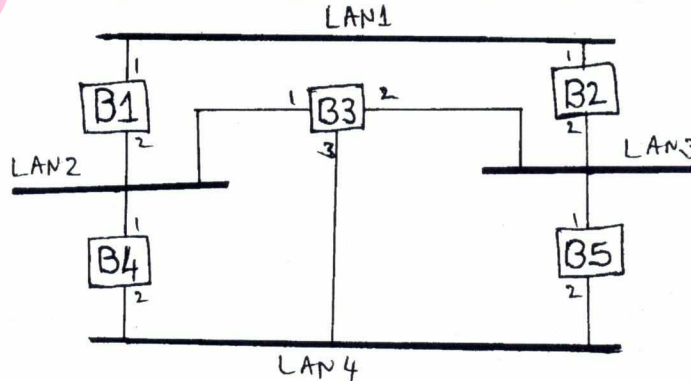

Fig.Q5(a)   **(10 Marks)**

b. Define repeater, bridge and router with necessary diagrams. **(06 Marks)**

c. Differentiate between a bus backbone network and star backbone network. **(04 Marks)**

6 a. An ISP is granted a block of addresses starting with 150.80.0.0/16. The ISP wants to distribute these blocks of 2600 customers as follows:
   i) The first group has 200 medium size business; each needs 16 addresses.
   ii) The second group has 400 small business; each needs 8 addresses.
   iii) The third group has 2000 households; each needs 4 addresses.
   Design the subblocks and give the slash notation for each subblock. Find out how many addresses ate still available after these allocations. **(10 Marks)**

b. Explain briefly strategies used to handle the transition from IPv4 to IPv6. **(06 Marks)**

c. A block of addresses is granted to a small organization. One of the addresses is 205.16.37.39/28. What is the first address, last address and number of address in the block. **(04 Marks)**

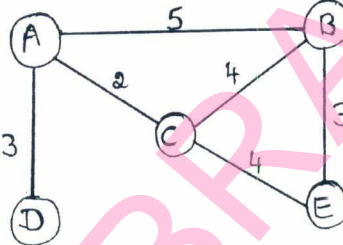7 a. Explain the 'Distance Vector Routing' for the following example shown in Fig.Q7(a).

Fig.Q7(a) **(10 Marks)**

b. Briefly discuss the following forwarding techniques:
   i) Next-Hop method versus Route method
   ii) Network-specific method versus Host specific method. **(06 Marks)**

c. Distinguish between multicasting and multiple unicasting. **(04 Marks)**

8 a. Explain connection establishment and connection termination in TCP. **(10 Marks)**

b. Write a note on DNS. **(06 Marks)**

c. Write a short note on source port number and destination port number in user datagram. **(04 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2013
Optical Fiber Communication

Time: 3 hrs.   Max. Marks:100

**Note: *Answer FIVE full questions, selecting
at least TWO questions from each part.***

PART – A

1 a. Discuss the advantages and disadvantages of OFC.   (06 Marks)
   b. Explain Mode Field Diameter (MFD) of a single mode fiber.   (06 Marks)
   c. Differentiate between glass fiber and plastic fibers. In case of glass fiber, how RI can be varied?   (04 Marks)
   d. A SI multimode fiber with a NA of 0.20 supports approximately 1000 modes at an 850nm wavelength.
     i)   What is the diameter of its core?
     ii)   How many modes does the fiber support at 1320 nm?
     iii)   How many modes does the fiber support at 1550 nm?   (04 Marks)

2 a. Explain the "pulse dispersion" with suitable diagram and differentiate MMSIF, MMGIF and SMF by their information carrying capacity with reason.   (06 Marks)
   b. Discuss the following for optical fibers:
     i)   Extrinsic absorption.
     ii)   Material dispersion.   (08 Marks)
   c. Optical power launched into fiber at transmitter end is 150μw. The power at the end of 10km length of the link working in first window is -38.2 dBm. Another s/m of same length working in second window is 47.5 μw. Same length s/m working in third window has 50% of launched power. Calculate fiber attenuation for each case and mention wavelength of operation.   (06 Marks)

3 a. A double-hetero junction "InGaAsP" LED emitting at a peak wavelength of 1310 nm has radiative and non radiative recombination times of 25 ns and 90 ns respectively. The drive current is 35 mA.
     i)   Find the internal quantum efficiency and the internal power.
     ii)   If the RI of the light source material is n = 3.5. Find the power emitted from the device.   (06 Marks)
   b. Describe the following terms relating to LASER:
     i)   External quantum efficiency.
     ii)   Wavelength spacing.   (06 Marks)
   c. Explain the three factors which affects the response time of a photodiode.   (08 Marks)

4 a. Discuss the different lensing scheme used to improve the source-to-fiber coupling efficiency, with the necessary sketches.   (06 Marks)
   b. For a surface emitting LED has radiance of 150W/(cm^2.sr) and radius of emitting area is 35μm. Calculate the optical power coupled to the fibers with
     $a_1 = 25$μm and NA = 0.20, step index
     $a_2 = 50$μm and NA = 0.20, step index.   (06 Marks)
   c. Define fiber splicing. Explain different types of splicing with neat sketches.   (08 Marks)

PART – B

5 a. Explain the different types of front-end amplifiers in optical receiver. (06 Marks)
   b. With a neat sketch, explain how system performance information can be obtained from the eye diagram. (08 Marks)
   c. Write a short note on burst-mode receivers. (06 Marks)

6 a. Following are the parameters of a point-to-point optical link:
      i)   Optical power launched   : +3dBm
      ii)   Sensitivity of detector   : -32dBm
      iii) Source/detector connector loss   : 1dB
      iv)   Length of optical cable   : 60 km
      v)   Cable attenuation   : 0.3dB/km
      vi)   Jumper cable loss   : 3dB
      vii) Connector loss at each fiber   : 1dB
            joint (two at each transmitter and receiver
            end because of the jumper cables)
      Compute the power margin of the link using spread sheet method. (06 Marks)
   b. Explain the basic elements of analog link with different noise contribution. (09 Marks)
   c. What is sub carrier multiplexing? Explain. (05 Marks)

7 a. Explain the need of isolator in optical network. Give its principle of operation also. (06 Marks)
   b. Explain the operational principle and implementation of WDM. (08 Marks)
   c. Briefly discuss dielectric thin-film filters. (06 Marks)

8 a. Explain the three main optical amplifier types. (06 Marks)
   b. Describe:
      i)   SONET/SDH rings.
      ii)   SONET/SDH networks.
      iii) Frame format of STS-1 SONET. (10 Marks)
   c. An EDFA amplifier produces $P_{s,out}$ = 27dBm for an input $P_{s,in}$ = 2dBm at 1542 nm.
      i)   Find the amplifier gain, G.
      ii)   What is the minimum pump power required. (04 Marks)

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Seventh Semester B.E. Degree Examination, June / July 2013
Power Electronics

Time: 3 hrs.   Max. Marks:100

Note: 1. *Answer any FIVE full questions, selecting*
atleast TWO question from each part.
2. *Draw neat diagram and Waveforms, wherever possible.*

PART – A

1   a. What is Power Electronics? Draw a neat block diagram of generalized power converter system. State the applications of power electronics. **(06 Marks)**
    b. With neat circuit diagram and waveforms, explain the types of power electronic circuits. **(12 Marks)**
    c. Compare General – purpose, Fast recovery and Schokky diodes. **(02 Marks)**

2   a. The maximum junction temperature of a transistor is $T_J = 150^0C$ and the ambient temperature is $T_A = 25^0C$, If the thermal impedances are $R_{JC} = 0.4^0C/W$, $R_{es} = 0.1^0C/W$, and $R_{SA} = 0.5^0C/W$. Calculate   i) the maximum power dissipation and   ii)   the case temperature. **(04 Marks)**
    b. With the help of parasitic model and switching model, explain the switching waveforms of n – type (enhancement) MOSFET. **(10 Marks)**
    c. Write a note on isolation of gate and base drives. **(06 Marks)**

3   a. Using a two transistor model of thyristor, show that $I_A = \dfrac{\alpha I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$. **(06 Marks)**
    b. With neat sketch, explain turn – on characteristics of SCR. **(06 Marks)**
    c. The input voltage Fig. Q3(c) is $V_s = 200V$ with load resistance of $R = 5\Omega$. The load and stray inductances are negligible and the thyristor is operated at a frequency of $f_s = 2KHz$. If the required dv/dt is 100 V/μS and the discharge current is limited to 100A. Determine   i)   the values of R_s and C_s ii)   the snubber loss, and   iii)   the power rating of the snubber resistor. **(08 Marks)**
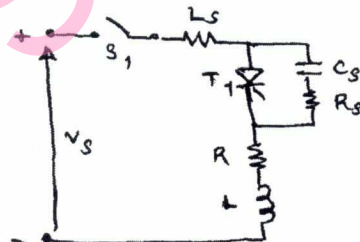

Fig.Q3.c. dv/dt protection circuit

4   a. Discuss the effect of inductance using the 1 - φ full converter. **(08 Marks)**
    b. What is phase control? Explain the principal of phase control using 1 - φ half wave controlled rectifier. **(08 Marks)**
    c. Compare circulating and non – circulating mode of operation of dual converter. **(04 Marks)**

PART – B

5 a. A thyristor circuit is shown in fig. Q5(a), if thyristor T_1 is switched on at t = 0, determine the conduction time of thyristor T_1 and the capacitor voltage after T_1 is turned off. The circuit parameters are L = 10μH, C = 50μF and V_s = 200V. The inductor carries an initial current of I_m = 250A. **(10 Marks)**
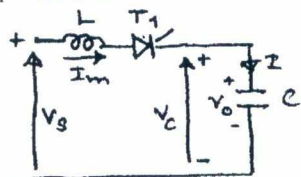

Fig. Q.5a: Self Commutated circuit.

   b. What is the principle of complementary commutation? Explain the same with the help of suitable circuit and waveforms. **(10 Marks)**

6 a. What is the principle of on off control? Explain the same with a single phase full – wave controller. **(06 Marks)**

   b. Draw a neat sketch of 1 - φ AC voltage controller with RL load and explain its working. **(06 Marks)**

   c. A single – phase full wave AC voltage controller has a resistive load of R = 10 Ω and the input voltage is V_s = 120V (rms), 60Hz. The delay angles of thyristors T_1 and T_2 are equal $\alpha_1 = \alpha_2 = \pi/2$. Determine i) the rms output voltage V_o ii) the input power factor PF iii) the average current of thyristor I_A and iv) the rms current of thyristor I_R. **(08 Marks)**

7 a. With a neat circuit diagram, explain the operation of a step down chopper and also explain constant frequency and variable frequency operation. Derive an expression for output voltage incase of step down chopper. **(10 Marks)**

   b. A step – up chopper with a pulse width of 200μs operating on 200V, dc supply. Calcualte the output voltage, if the blocking period of the device is 50μs. **(02 Marks)**

   c. With a neat circuit diagram and quadrant operation, explain class E chopper. **(08 Marks)**

8 a. With a neat circuit diagram, of 1 - φ half bridge inverter, explain the principle of operation of an inverter. **(08 Marks)**

   b. Write brief note on current source inverter. **(06 Marks)**

   c. With the help of circuit diagram and waveforms, explain a variable DC – link inverter. **(06 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2013
DSP Algorithms and Architecture

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1. a. List and explain the issues that have to considered in designing and implementing a DSP system. **(04 Marks)**

   b. Implement an FIR filter for $y(n) = \dfrac{(x(n) + x(n-1) + x(n-2))}{3}$. Determine the (i) system function (ii) magnitude response function (iii) phase response function. Plot its magnitude and phase response. **(06 Marks)**

   c. Explain the process of decimation. **(04 Marks)**

   d. The signal sequence $x(n) = [0 \quad 2 \quad 4 \quad 6 \quad 8]$ is interpolated using the interpolation filter sequence $b_k = [0.5 \quad 1 \quad 0.5]$ and the interpolation factor is 2. Determine the interpolated sequence $y(m)$. **(06 Marks)**

2. a. Explain the different frequently used techniques to prevent overflow and underflow conditions occurring in MAC unit. **(04 Marks)**

   b. Explain the different ways in which the on-chip memory can be organized efficiently and cost-effective manner. **(04 Marks)**

   c. Explain the register pointer updating algorithm for circular buffer addressing mode. **(04 Marks)**

   d. List the techniques used in DSP architecture to increase speed of operation and operations that should be accomplished in single clock to achieve parallelism in DSP iomplementation. **(08 Marks)**

3. a. Explain with a neat clock diagram the indirect addressing mode of TMS320C54XX processor. Give the operand syntax and operation for the following:
   i) Circular addressing mode   ii) Bit reverse addressing mode. **(10 Marks)**

   b. Explain the different ways in which PC addresses the program memory either on-chip or off-chip and gets loaded for execution of instructions. **(06 Marks)**

   c. Specify the on-chip memory configuration for $MP/\overline{MC}$, OVLY and DROM located in processor mode status register of 5416 processor. **(04 Marks)**

4. a. Describe the operation and application of the following instructions of TMS320C54XX processor with example:
   i) MAC   ii) MAS   iii) LD *AR4, 4, A
   Given contents of AR4 is 8boeh& S×M = 1. Determine the contents of accumulator. **(06 Marks)**

   b. Write an ALP of TMS320C54XX processor to compute
   $y(n) = h \cos x(n) + h(1) x(n-1) + h(2) x(n-2)$, using MAC instruction, where h(0) = 5, h(1) = 31, h(2) = 13 are in program memory locations starting at h. x(n) = 1, x(n – 1) = 5 x(n – 2) = – 3 are in data memory locations starting at x.y(n) is to be saved (lower 16 bits) in location y and y +1 (higher 16 bits). **(05 Marks)**

   c. With a neat sketch, describe the Host port interface signals. **(04 Marks)**

   d. Explain the six-stage pipelined execution of TMS320C54XX. **(05 Marks)**

PART – B

5   a.   Define Q Notation. Explain Q_7 and Q_{15} Notations with example.   (05 Marks)

b.   Realize and write a program for a second order IIR filter on TMS320C54XX   processor defined by the transfer function $H(z) = \dfrac{0.104 - 0.102z^{-1} + 0.104z^{-2}}{1 + z^{-1} - 0.612z^{-2}}$.   Assume that the filter coefficients are q_{15} numbers x(n) is the input sample (integer), input samples are placed in buffer, insamples, from a data file, data_in.dat. y(n) is computed output. The output samples are placed in a buffer outsamples.   (10 Marks)

c.   Explain with necessary block diagram, memory organization for implementing FIR filter of order N.   (05 Marks)

6   a.   Determine the following for a 512 point FFT computation :
i) Number of stages   ii) Number of butterflies in each stage   iii) Number of butterflies needed for the entire computation. iv) Number of butterflies that need no twiddle factors. v) Number of butterflies that require real twiddle factors   vi) Number of butterflies that require complex twiddle factors.   (06 Marks)

b.   Explain how scaling prevents overflow conditions in the butterfly computation.   (06 Marks)

c.   Write a TMS320C54XX program segment that implements 8 point DIT FFT bit reversed index generation and to clear FFT data memory.   (08 Marks)

7   a.   Interface an 8k×16 program ROM to the C5416 DSP in the address range 7FE000h – 7FFFFFh.   (06 Marks)

b.   Explain with a flow chart diagram for software polling for the programmed I/O A/D converter interface.   (06 Marks)

c.   Define interrupt. Write a flow chart of interrupt handling by C54XX processor.   (08 Marks)

8   a.   Explain with neat block diagram the PCM 3002 interfaced to TMS320VC5416 in the DSK.   (06 Marks)

b.   Explain with block diagram the biotelemetry receiver implementation.   (06 Marks)

c.   With a neat sketch, explain the JPEG encoder and decoder.   (08 Marks)

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Seventh Semester B.E. Degree Examination, June/July 2013
Operating Systems

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1 a. Explain the primary concern of an O.S. **(06 Marks)**
   b. What are two popular strategies for resource allocation? Explain. **(08 Marks)**
   c. Explain the concepts and techniques used to optimize the throughput in a multiprogramming system. **(06 Marks)**

2 a. Explain with a schematic the working of a round robin scheduling with time slicing. **(06 Marks)**
   b. Explain two layered O.S. structure. **(07 Marks)**
   c. Explain microkernel based operating systems. **(07 Marks)**

3 a. Explain process states and fundamental state transitions for a process. **(08 Marks)**
   b. Define: i) Interacting process   ii) Control synchronization   iii) Race-condition iv) Data access synchronization. **(06 Marks)**
   c. Explain kernel level threads and user level threads. **(06 Marks)**

4 a. To perform memory allocation from a tree list, explain (i) First-fit technique (ii) Best-fit technique. **(06 Marks)**
   b. Explain the concept of memory protection using (i) Bound register (ii) Memory protection keys. **(08 Marks)**
   c. Make a critical comparison between contiguous and non-contiguous memory allocation. **(06 Marks)**

PART – B

5 a. Explain the technique of page faults and page replacement used in demand paging. **(06 Marks)**
   b. Describe the functions performed by the VM handler. **(06 Marks)**
   c. Show the behaviour of the FIFO page replacement policy for the following page reference and reference time for a program:
Page reference string: 5, 4, 3, 2, 1, 4, 3, 5, 4, 3, 2, 1, 5, ………..
Reference time string: t_1, t_2, t_3, t_4, t_5, t_6, t_7, t_8, t_9, t_{10}, t_{11}, t_{12}, ………..
Show how many page faults would occur for FIFO replacement assuming 3 and 4 frames. **(08 Marks)**

6 a. With a schematic explain the working of RAID. **(07 Marks)**
   b. Explain the indexed allocation of disk space. **(07 Marks)**
   c. Explain the interface between file system and ICOS. **(06 Marks)**

7   a. Explain long, medium and short-term scheduling in a time sharing operating system.

    (06 Marks)

    b. The following table gives the processes for scheduling:

Process	Arrival time	Execution time	Deadline
P_1	0	3	4
P_2	2	3	14
P_3	3	2	6
P_4	5	5	11
P_5	8	3	12

Calculate the mean turn around time and mean weighted turn around for
(i) FCFS scheduling   (ii) SJN scheduling.

    (08 Marks)

    c. Explain the process scheduling in UNIX.

    (06 Marks)

8   a. Explain primary issues in message passing.   **(06 Marks)**
    b. Explain about mail boxes. What are its advantages?   **(08 Marks)**
    c. Explain about interprocess communication in UNIX.   **(06 Marks)**

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Seventh Semester B.E. Degree Examination, June/July 2013

Real Time Systems

Time: 3 hrs.   Max. Marks:100

Note: *Answer FIVE full questions, selecting*
at least TWO questions from each part.

PART – A

1 a. Give two definitions for real time system. **(04 Marks)**
   b. Explain different classifications of RTS based on synchronization between external process and internal tasks of the computer. **(08 Marks)**
   c. Explain hard and soft RTS with relevant equations. **(08 Marks)**

2 a. Compare batch processing and continuous processing. **(05 Marks)**
   b. With a neat diagram, explain distributed systems with its advantages. **(10 Marks)**
   c. Write a note on supervisory control systems. **(05 Marks)**

3 a. The clock on computer generates an interrupt for every 20 ms. Draw a flow chart for interrupt service routine, which has to keep a 24 hour clock in terms of hours, minutes and seconds. **(08 Marks)**
   b. Explain a simple digital input and output interfaces. **(10 Marks)**
   c. Write a note on different LAN topologies. **(02 Marks)**

4 a. Explain scope and visibility of a variable. **(04 Marks)**
   b. What are the basic language requirements for RT language? Explain. **(10 Marks)**
   c. What is CUTLASS? What are the requirements of CUTLASS? **(06 Marks)**

PART – B

5 a. Explain different scheduling strategies. **(06 Marks)**
   b. Three cyclic tasks A, B, C are required to run at 1 tick, 2 ticks and 3 ticks respectively (1 tick = 20 ms). Assuming tasks A, B, C consumes 5 ms, 8 ms and 10 ms respectively. Write task activation diagram for priority order. (Context switching time = 0).
      i) A (highest), B, C   ii) B (highest), A, C **(06 Marks)**
   c. What is code sharing? Explain serially reusable and re-entrant code. **(08 Marks)**

6 a. With a neat diagram, explain the general structure of IOSS. **(07 Marks)**
   b. Explain the problem of shared memory. How semaphores are used to overcome this problem? **(09 Marks)**
   c. Explain Liveness. **(04 Marks)**

7 a. Explain foreground and background system with a flowchart. **(10 Marks)**
   b. Differentiate pool and channel. **(04 Marks)**
   c. Explain software design for RTS using software module. **(06 Marks)**

8 a. Explain functional specifications with respect to a drying oven. **(07 Marks)**
   b. Explain Yourdon methodology. **(05 Marks)**
   c. With a relevant diagram, explain Ward and Mellor's method. **(08 Marks)**

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